LOW VOLTAGE NON-VOLATILE MEMORY CELL

ABSTRACT

A memory cell comprises a multilayer gate heating structure formed over a channel region between source and drain regions. The multilayer gate heating structure comprises polysilicon and metal silicide layers stacked over a similarly shaped gate oxide. When a programming voltage is applied across the metal silicide layer, there is intense localized heating. The heating causes segregation of the channel dopant atoms towards the source and drain regions, lowering the threshold voltage of the device. The heating causes carrier activation in the polysilicon layer and dopant penetration through the oxide layer into the channel region, thereby increasing the threshold voltage of the device.